Integrated Coplanar MM-Wave Amplifier with Gain Control Using a Dual-Gate InP HEMT

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Abstract— **Variable gain mm-wave amplifiers, based on InP high-electron mobility transistor (HEMT) devices, are demonstrated. The two-stage circuits consist of a single-gate (SG) and dual-gate (DG) transistor. The influence of the gate recess depth on the gain control range is investigated. A maximum gain control range of 32 dB is achieved which is the largest reported in the mm-wave range for a monolithically integrated variable gain amplifier (VGA). The maximum gain is 25.7 dB at 48.5 GHz with a 3-dB bandwidth of 10.5 GHz. The circuits were fabricated in coplanar technology.**

I. Introduction

MICROWAVE systems are advancing toward mm-wave frequencies because of the need for higher data rates which in turn require large bandwidths. Wireless applications are also planned in the mm-wave range because of a limited number of available frequency bands at lower frequencies. Furthermore, the high attenuation in the air at mm-wave frequencies can be advantageous for the efficient use of allocated frequencies (e.g., multiple use of the same frequency bands within a building). In such microwave systems, the variable gain amplifier (VGA) is an essential component for controlling the power of the transmitted and received signals. In monolithic-microwave integrated amplifiers, gain control has been realized by controlled feedback or dual-gate (DG) cascode FET's. For mm-wave frequencies, however, feedback can cause stability problems. In this case, the DG high-electron mobility transistor (HEMT) offers an attractive alternative for gain control. An added advantage of the cascode circuit is that it has a high reverse isolation. VGA's have been demonstrated up to 20 GHz [1]–[4]. In the mm-wave range, little has been published on VGA's [5]. This work demonstrates monolithically integrated two-stage VGA's for the frequency range 25–50 GHz. The second stage uses a DG InP HEMT device to control the gain. The influence of the gate recess depth was investigated.

II. Fabrication

The single-gate (SG) and DG HEMT devices with $0.2{\cdot}150\,\mu m^2$ T-gates were fabricated on an AlInAs/GaInAs/InP structure grown by MBE. The T-gates of both devices are defined by direct-write electron-beam lithography using a three-layer resist system [6]. The T-gates of the DG HEMT are separated by $1.4\,\mu m$. Fig. 1 shows the current gain (h_{21}) and the maximum available gain (MAG) for both SG and DG devices. The SG transistor has the higher current gain whereas the cascode device has higher maximum available gain and maximum stable gain due to the lower output conductance.

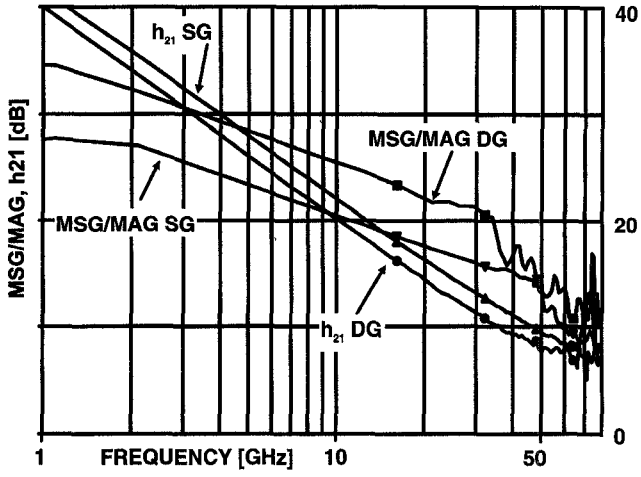

Fig. 1. Current gain (h_{21}) and maximum available gain (maximum stable gain, respectively) for an SG and a DG HEMT.

The use of coplanar technology simplifies the process since no wafer thinning nor via holes are required. To suppress any parasitic slotline mode on the coplanar waveguide (CPW), bond wires are used to connect the ground planes. A photograph of the circuit is shown in Fig. 2. The chip area is only 1.9×1.3 mm^2. This could be further reduced by optimizing the bias and matching networks.

Two samples were fabricated with different gate recess depths to investigate the process influence on the amplifier characteristics; sample A with a deep gate recess, i.e., a threshold voltage of -0.9 V, and sample B with a shallow gate recess and a more negative threshold voltage.

III. Design

The mm-wave amplifier consists of two stages (Fig. 3). The first stage is a common source HEMT device. The second stage is a DG HEMT in a cascode configuration where gate 3 is RF-grounded. The advantages of the DG device are higher gain, lower feedback, and the possibility to vary the gain.

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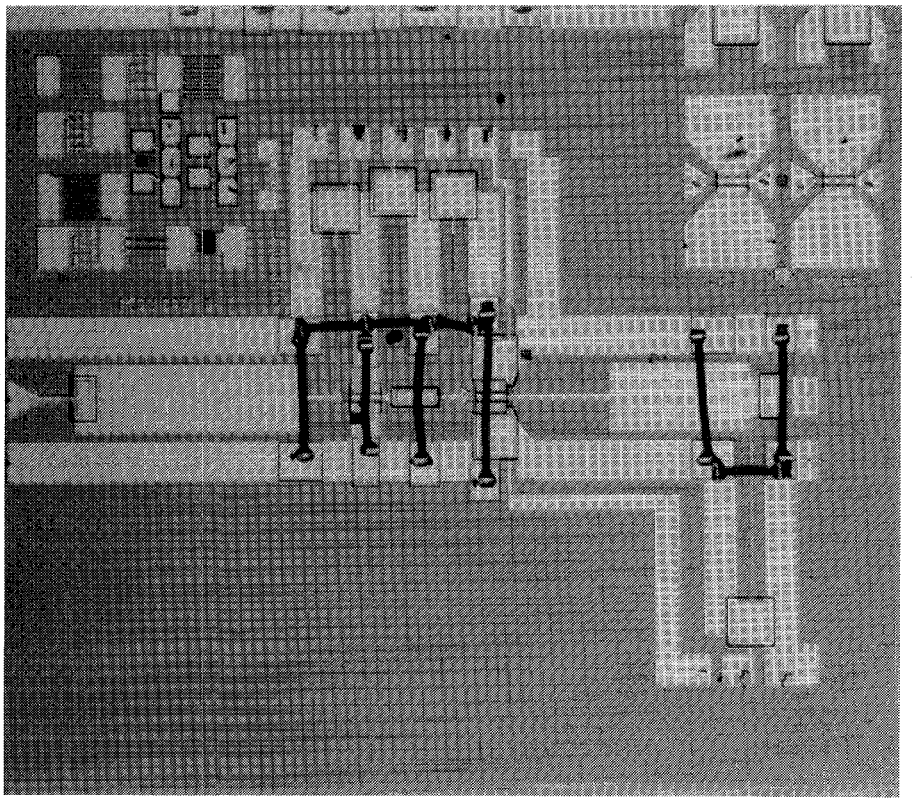

Fig. 2. Photograph of the DG mm-wave HEMT amplifier (chip size: 1.9 × 1.3 mm^2).

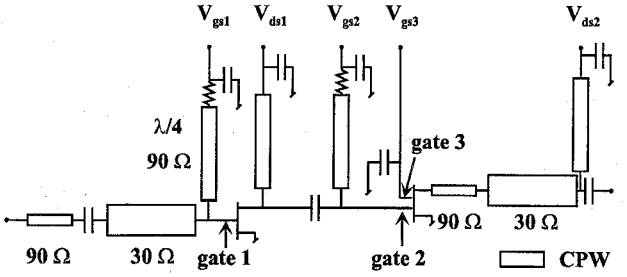

Fig. 3. Circuit schematic of the fabricated DG HEMT amplifier.

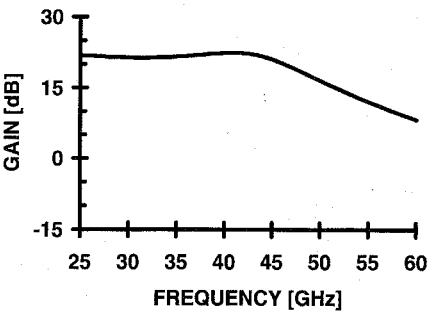

Fig. 4. Simulated amplifier gain when biased for maximum gain.

The gain is controlled by the dc gain control voltage V_{gs3} applied to gate 3. When the gain control voltage becomes more negative, the current and gain decrease. The amplifier was designed for maximum gain and a wide range of gain variation. Series coplanar transmission lines (CPW) were used as matching networks. The bias is applied on-chip through $\lambda/4$ transmission lines which are RF-shorted with MIM capacitors. The dc-blocking capacitors are also on-chip.

The HEMT small-signal model used for the simulations in TOUCHSTONE is described in [7]. The S-parameters of the bias lines and T-junctions were calculated with an electromagnetic "3-D planar" simulator. This was necessary to take into account the parasitic capacitances and inductances originating at the T-junctions and coupling between the bias lines. These effects are not included in the TOUCHSTONE CPW models. The components were inserted into the simulation as S-parameter data files. To reduce the coupling, the bias lines could be covered by air bridges. Fig. 4 shows the simulation of the gain when the circuit is biased for maximum gain.

Stability is a critical issue in multistage amplifier circuits. Therefore, each stage was carefully analyzed for stability by plotting the k-factor and stability circles. It was found that 40-Ω resistors in the gate bias lines were necessary to ensure the stability of the entire circuit.

IV. Measurements and Results

The DG HEMT amplifiers were fully characterized by the measurement of the S-parameters, third-order intercept point (IP3), and noise figure. The circuits were also tested for oscillations using a spectrum analyzer. No oscillations were observed over the whole possible bias range. The S-parameters were measured from 0.1–78 GHz with an HP8510C and an HPV85104A mm-wave extension. The calibration

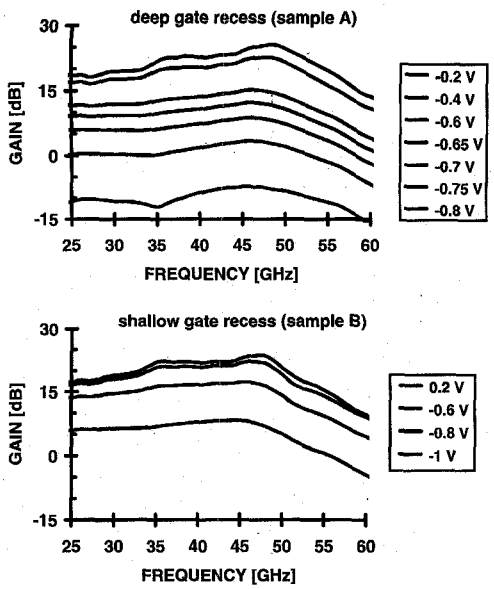

Fig. 5. Measured gain of the two samples with the deep and shallow gate recess depths for different gain control voltages V_{gs3} (V_{ds1} = 1.5 V and V_{ds2} = 2 V).

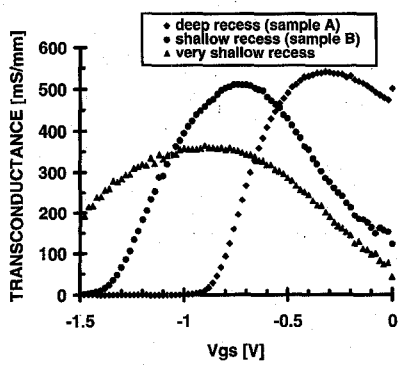

Fig. 6. Transconductance versus gate source voltage for three different gate recess depths.

method used was LRRM [8]. To prevent compression of the measured amplifiers, low power levels and attenuators had to be used. Fig. 5 shows the gain of circuits fabricated with deep (sample A) and shallow (sample B) gate recesses for different gain control voltages V_{gs3}. The maximum gain is 25.7 dB at 48.5 GHz with a 3-dB bandwidth of 10.5 GHz and a controllable gain range of 32 dB for the device with the deeper recess. The measured S_{12} is less than -32 dB. The device with the shallower gate recess has a maximum gain of 23.8 dB, but the gain control is less effective. For the same gain control voltage change, the gain control range is much smaller. To confirm the assumption that the gain control range depends on the gate recess depth, further investigations were carried out. Fig. 6 shows the transconductance of SG HEMT devices for different gate recess depths. It can be seen that the maximum transconductance and shape of the curves depend on the gate recess depth. The devices with the deeper gate recess have the maximum transconductance at a more positive gate voltage, and the voltage difference between maximum transconductance and pinchoff is smaller. This can

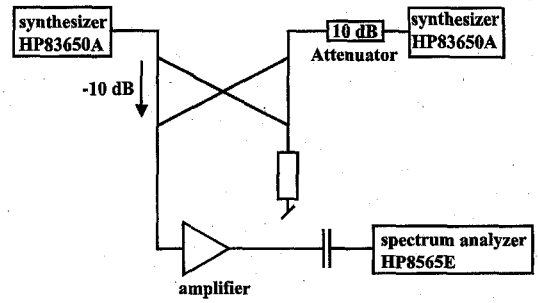

Fig. 7. Measurement setup for the IP3 measurement.

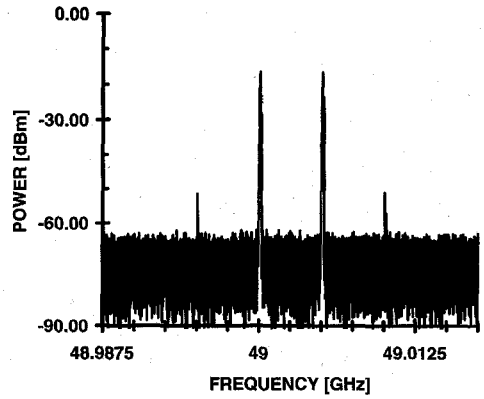

Fig. 8. Measured spectrum with two input frequencies at 49 GHz and 49.005 GHz.

be attributed to the shorter distance between the gate and the channel which results in a more efficient modulation of the carriers in the channel. In the DG HEMT, reducing the drain current leads to a lower gain, up to the point where the device is pinched off. As a result, a relatively small change of the gain control voltage V_{gs3} is sufficient to cover the entire gain control range when a deep gate recess is used. On the other hand, the circuit with the shallow gate recess requires a larger control voltage change and a more negative control voltage. If the gate recess were even shallower (third curve, Fig. 6), the full gain control range could not be used since breakdown would occur before the channel became fully depleted. To determine the optimum gate recess depth, one has to consider the gain control range and the maximum gain, which also depends on the gate recess depth. Experiments show that a deeper gate recess than sample A would reduce the gain.

The measurement setup for the determination of the IP3 is shown in Fig. 7. It is important to have high isolation between the two synthesizers which is achieved by a 10-dB directional coupler and internal and external attenuators. Both synthesizers were first connected directly to the spectrum analyzer to verify that there was no intermodulation of the signals. Furthermore, the signal power at the input of the spectrum analyzer had to be low enough to prevent intermodulation originating at the analyzer. The applied signals have a frequency difference of 5 MHz. The IP3 was calculated using the following formula: IP3 = S + dBc/2 where S is the signal power of one signal in dBm, and dBc is the intermodulation product level compared to the carrier in dB [9]. The signal power S was measured

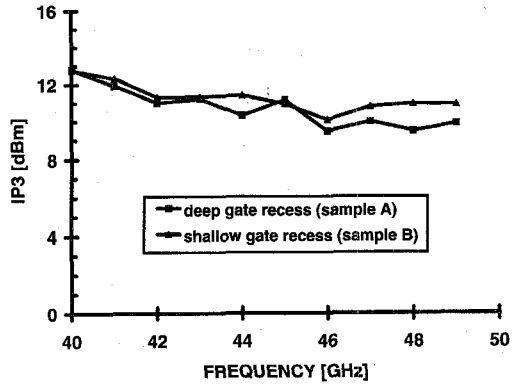

Fig. 9. IP3 versus frequency at a maximum gain bias.

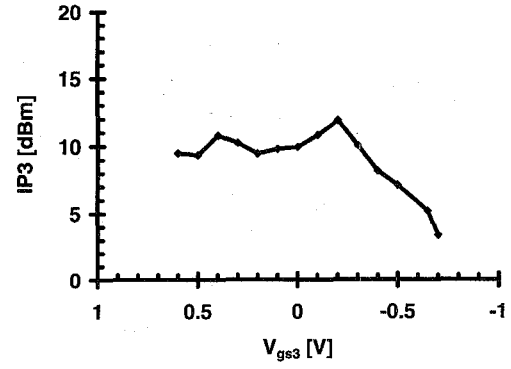

Fig. 10. IP3 versus gain control voltage V_{gs3} at 49 GHz.

with a power meter. A typical spectrum is shown in Fig. 8. The two input signals at 49 GHz and 49.005 GHz can be seen as well as the third-order intermodulation signals. Higher order intermodulation cannot be detected. The IP3 versus frequency plot of both chips show a decrease in the IP3 of 3 dB between 40–50 GHz (Fig. 9). The minimum IP3 is 9.5 dBm for the circuit with deeper gate recess (sample A) and 10 dBm for the other circuit. There is no significant difference in the IP3 for the two recess depths. The ripple is introduced by the measurement setup (e.g., no correction of the reflections between the amplifier and synthesizers). The IP3 is plotted against the gain control voltage V_{gs3} in Fig. 10 for the deeper recessed sample (A) at 49 GHz. The IP3 is approximately 9.5 dBm at a maximum gain bias and decreases for $V_{gs3} = -0.7$ V to 3.5 dBm. For applications demanding constant output power, the limiting IP3 is at a minimum gain bias, i.e., negative gain control voltage V_{gs3}, whereas for constant input power, the limiting IP3 is at a maximum gain bias.

Fig. 11 shows the measured noise figure between 25–42 GHz [10]. The noise figure is 4.5 dB at 42 GHz. The observed ripple in the noise figure curve is due to the fact that the impedance of the noise source is not exactly 50 Ω.

Table I shows a comparison between this work and previous amplifiers from Kashiwa [5]. These results compare favorably with [5], although in that work the amplifiers consisted of two cascaded low-noise amplifier (LNA) monolithic-microwave integrated circuits (MMIC's); an LNA and a VGA. With only a two-stage circuit, a higher gain and a higher gain control range could be achieved, and the chip area could be reduced.

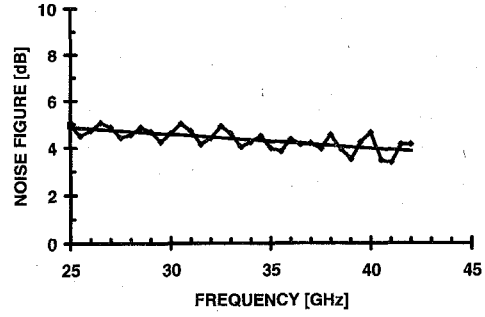

Fig. 11. Noise figure of the VGA.

TABLE I
COMPARISON BETWEEN PREVIOUS AND THIS WORK

	[5]	**This work**
technology	GaAs pHEMT	**InP HEMT**
stages	3	**2**
gain [dB]	24.5	**25**
gain control range	30 [dB]	**32 [dB]**
IP3 [dBm]	-	**9.5**
frequency range [GHz] (3 dB bandwidth)	ca. 41-52.5	**41.3-51.8**
chip area [mm^2]	6.8	**2.5**
noise figure [dB] @ 42 GHz	1.8	**4.5**

V. CONCLUSION

Two-stage mm-wave VGA's with different gate recess depths were fabricated. An optimum gate recess depth was found resulting in a VGA with a maximum gain of 25.7 dB and gain control range of 32 dB. This is the highest gain control range reported for a mm-wave MMIC based on InP HEMT devices. The variable gain is achieved using a DG HEMT in the second stage. The gain control range could be further improved by incorporating a DG transistor in the first stage. As well as providing gain control, the DG HEMT improves the isolation (>32 dB) from the output to the input. An IP3 larger than 9.5 dBm was measured.

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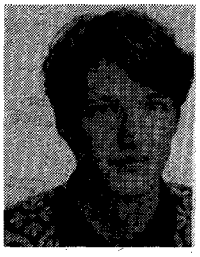
H.-P. Meier, photograph and biography not available at the time of publication.



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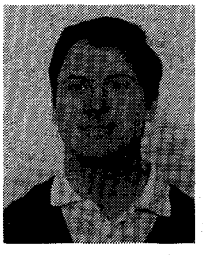

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